REMARKS

Claims 1-40 are currently pending. Claims 4 and 23 have been allowed. Applicants have amended claims 1, 5, 6, 8, 11, 19, 24, 25, and 30 to clarify applicants' invention. Applicants have canceled claims 7, 26, and 37-40. No new matter has been added.

I. Interview Summary

Applicants thank the Examiner for the courtesy of the in-person interview conducted on January 23, 2007. Applicants' representatives, Stephen Bishop and Dongyun Lee (Sr. Design Manager for Silicon Image) attended the interview. During the interview, proposed claim amendments were discussed, as were portions of the specification and drawings including Figures 30 and 31. Mr. Bishop pointed out examples of claim limitations present in independent claims 1 and 19 that were not present in Sonnier et al., Davidsson et al. and Knecht et al. No other references were discussed. Examiner Kim agreed to consider the applicants' arguments if presented in a formal response.

II. Restriction Requirement

In the Office Action, the Examiner withdrew claims 37-40 from consideration as being directed to a non-elected invention. Applicants have canceled claims 37-40 and reserve the right to pursue the subject matter of such claims in a divisional.

III. Objections to the Specification

The Examiner has objected to the title of the invention as not being descriptive. Applicants have amended the title to address the Examiner's concerns.

In response to the Examiner's request, applicants have updated the status of the related U.S. patent applications contained in the CROSS-REFERENCE TO RELATED APPLICATIONS section.

IV. 35 U.S.C. §103 Claim Rejections

The Examiner has rejected certain claims under 35 U.S.C. §103(a) as follows:

Claim Nos.	*Combination of References*
1, 2, 5-8, 10-21 and 24-36	Sonnier et al., Davidson et al., and Knecht et al.
3 and 22	Sonnier at al., Davidson et al., Knecht et al., and Jeong et al.
9	Sonnier at al., Davidson et al., Knecht et al., and Lee

Applicants respectfully disagree with the Examiner's characterization of these references. Applicants have, nevertheless, amended independent claims 1 and 19 to recite that the memory in applicants' memory device is comprised of "a plurality of banks," that the plurality of serial ports facilitate "accessing the plurality of banks," and that a switch is provided for "selectively routing symbols between the plurality of ports and the plurality of banks, wherein the bits of symbols are routed by the switch in parallel." Sonnier and the other cited references fail to disclose or teach such a structure. As depicted in Figures 1A and 1C, Sonnier discloses separate memory systems 28 that are contained in CPUs 12A and 12B. Router 14A allows packets to be routed to the separate memory systems, such as the first memory system contained in CPU 12A or the second memory system contained in CPU 12B. (Sonnier, 11:12-21.) Ports on the router allow I/O packet interfaces 16 to communicate with the CPUs. (Id., 10:36-43.)

Applicants' architecture differs from that disclosed in Sonnier in a number of respects. First, applicants' architecture uses a port to access a bank within a memory, whereas Sonnier teaches using a port to access different memories. From an implementation standpoint, such a distinction is important as Sonnier teaches scaling by adding additional memory devices. For example, Sonnier discloses extending the

configuration of the system by replicating the sub-processor systems. (Sonnier, 12:37-47.) In contrast, applicants' architecture allows scaling using a single memory. It would not have been obvious to modify Sonnier to use a single memory since Sonnier teaches away from applicants' solution. Second, applicants' architecture receives data serially at the plurality of ports, but switches data in parallel. In contrast, Sonnier discloses receiving and switching data in parallel. (Id., 11:29-32, describing that theTNet Links L are bit-parallel links.)

Applicants also reiterate their previous argument that the various combinations of Sonnier, Davidsson, Knecht, Jeong and Lee appears to be a mere patching together of the prior art using applicants' specification as a template. Such a rejection is improper under the current standard that demands a "teaching, suggestion, or motivation" to combine prior art references in a §103 rejection. (See, e.g., ARGUMENTS FOR PRE-APPEAL BRIEF REVIEW submitted May 10, 2006.)

V. Conclusion

For the reasons set forth above, applicants request that the outstanding rejections be withdrawn. Note that by focusing on specific claims and claim limitations in the discussion above, applicants do not intend to imply an agreement with the Examiner's assertions regarding other claims and claim limitations. If the Examiner has any questions or believes a telephone conference would expedite prosecution of the application, the Examiner is encouraged to call the undersigned at the number below.

Applicant has included payment by EFT Account No. SEA1PIRM of $120.00 to cover the fee for the Petition for Extension of Time. Should there exist any deficiency in fees due, please charge our Deposit Account No. 50-0665, under Order No. 594728812US from which the undersigned is authorized to draw.

Dated:

23 February 2007

Respectfully submitted,

By _____

Stephen Bishop
Registration No.: 38,829
PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-3129
(206) 359-7198 (Fax)
Attorneys for Applicant